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09/475,452	12/30/1999	ANAND MURTHY	042390.P7794	6341

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EXAMINER
LEE, EUGENE

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/475,452	MURTHY ET AL.
	Examiner	Art Unit
	Eugene Lee	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 8/19/02 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/475,452 is acceptable and a CPA has been established. An action on the CPA follows.

Drawings

2. FIG. 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C.

122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 8, 9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Krivokapic '587. Krivokapic discloses (see, for example, FIG. 2p) a transistor (MOS device) 300 comprising a substrate (first conductivity region) 201, gate oxide (gate dielectric) 208, gate (gate electrode) 210, spacer (sidewall spacers) 219, source 217 and drain 218. The distance between the source and drain define a channel wherein the distance directly beneath the gate electrode is larger than the distance deeper into the substrate. Regarding claim 12, see, for example, column 9, lines 19-40 and element 241.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9 and 12 above, and further in view of Takeuchi '351. Krivokapic does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric. However, Takeuchi teaches (see, for example, FIG. 11 (c)) a MOSFET comprising elevated source and drain regions 7B comprising a facet. In column 12, lines 45-63, Takeuchi teaches that such a structure provides reduced parasitic

capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use this structure in Krivokapic's invention in order to reduce parasitic capacitance.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9 and 12 above, and further in view of Choi '582. Krivokapic does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film of Choi in Krivokapic's invention in order to reduce hot carrier effects.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi '582. Krivokapic in view of Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film of Choi in Krivokapic in view of Takeuchi in order to reduce hot carrier effects.

9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9 and 12 above, and further in view of Choi et al. '088. Krivokapic does not disclose a pair of deposited silicon or silicon alloy regions having a first conductivity type formed between said pair of deposited silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region. However, Choi (see, for example, FIG. 2 and FIG. 3) a structure 106 comprising halo regions 120, 122. Choi teaches that halo regions provide higher punchthrough voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use halo regions in order to attain a higher punchthrough voltage.

10. Claims 7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587. Krivokapic does not disclose an inflection point which occurs between 50-200 A laterally beneath said gate electrode and at a depth of between 25-200 A beneath said gate dielectric. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these depths, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 10 and 11, Krivokapic does not disclose the concentration of said deposited silicon or silicon alloy source/drain regions of a second conductivity type having a concentration between 1X1018 / cm3 – 3X1021/ cm3 or approximately 1X1021 / cm3. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these concentrations, since it has been held that where the general conditions of

a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9 and 12 above, and further in view of Pfiester '315 and further in view of Takeuchi '351. Krivokapic does not disclose silicon-germanium alloy source/drain regions. However, Pfiester discloses (see, for example, column 6, lines 15-30 and column 12, lines 35-42) that combining silicon with germanium will improve electrical conductance. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to combine silicon and germanium in the source/drain regions of Krivokapic in order to improve the electrical conductance of the transistor.

Krivokapic in view of Pfiester does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric. However, Takeuchi teaches (see, for example, FIG. 11 (c)) a MOSFET comprising elevated source and drain regions 7B comprising a facet. In column 12, lines 45-63, Takeuchi teaches that such a structure provides reduced parasitic capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use this structure in Krivokapic in view of Pfiester in order to reduce parasitic capacitance.

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 in view of Pfiester '315 in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi '582. Krivokapic in view of Pfiester in view of Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edges of said gate electrode than the gate

dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film in order to reduce hot carrier effects.

Response to Arguments

13. Applicant's arguments filed 8/19/02 have been fully considered but they are not persuasive. FIG. 2p clearly shows the source/drain regions 217/218 curved inwardly beneath a gate 210 and gate oxide 208. From FIG. 2o, the point of the source and drain regions which are closest together resides beneath the gate 210 and gate oxide 208. Regarding claims 3 and 4, since the claims are directed to structure, the only important limitation in Choi is the structural limitation of a thicker gate dielectric. Therefore, since Krivokapic and Choi deal with the same semiconductor art (transistors) and gate oxide layers, the combination of Krivokapic and Choi is proper.

Applicant's arguments with respect to claims 13 and 14 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
September 22, 2002

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